ABSTRACT

In this paper a new low power flip-flop called Double-edge triggered Modified Hybrid Latch Flip-Flop (DMHLFF) has been proposed and compared to previous flip-flops. DMHLFF is a low power, low area, and fast flip-flop. Power consumption is reduced by avoiding unnecessary internal node transition. Power consumption in clock tree is also reduced by decreasing the frequency of clock to half of the clock frequency in single edge triggered flip-flop for the same throughput. These capabilities are obtained by modifying the structure of conventional Hybrid Latch Flip-Flop without any penalty in area. Reducing the number of transistor in stack leads to having less delay and thus higher operational speed compared to others flip-flops.

Keyword: low power, Edge-triggered flip-flop, node transition, LFSR.

1. INTRODUCTION

Power consumption of circuit and system is critically important in modern VLSI especially for low power application. Power optimization techniques are applied in different levels of digital design. Designing low power logic is one of the most important tasks to achieve this aim. Latch and flip-flop is critical to performance of digital system [1, 2]. It is widely used in memory design and test applications. There are some concerns in design of DFF such as \( T_{clk-q} \) (delay from \( clk \) to output of DFF), \( C_{clk} \) (load capacitance of the clock). These parameters, as well as the frequency of clock and the power consumption of the rest transistors in gate determine the performance of DFF. Reducing the \( C_{clk} \) or the frequency of clock has a great impact on the power consumption of clock tree and total power consumption of logic but reduces the operational frequency [8].

DFF is the main element of scan chain widely used in testing of digital circuit. Built-In Self-Test (BIST) is another practical solution in today’s complicated testing of digital systems. Usually, Linear Feedback Shift Register (LFSR) is used in test pattern generator and compressor units in BIST applications. LFSR is constructed of DFF and some XOR gates. Area overhead is one of the main concerns of test circuit. Reducing the area of DFF leads to reduction in overall test circuit’s area and hence, increasing the efficiency of BIST application. Power consumption of FF, during test is also a challenge as test patterns are highly irregular and may cause excessive power dissipation during test [3, 4]. Several efforts have been done to improve the performance of flip-flop. Some of the best previous works is reviewed here briefly.

Hybrid Latch Flip-Flop (HLFF) has been proposed based on generating explicit transparency...
window where the transition is allowed [5]. HLFF is a static, single edge-triggered FF. Existence of redundant transition in internal node in HLFF indicates more power consumption. It is similar to latch because it can provide a soft clock edge which allows for slack passing and minimize the effect of clock skew on cycle time [6].

Semi-Dynamic Flip-Flop has been known as fast flip-flop [7]. It is a single edge-triggered FF and faster than HLFF. Existence of 1-1 glitch leads to wasting of power. The number of transistors in this logic is greater than that of HLFF.

Conditional Capture Flip-flop (CCFF) has been proposed to reduce redundant transitions at internal nodes [8]. The conditional capture technique needs many additional transition for certain flip-flops which itself cause extra power consumption.

The power consumption in clock tree is depends on frequency, Voltage swing, and the load of clock tree [9]. If the sampling of input is performed in both rising and falling edge of clock (Double edge triggered) then, for same application and operational speed, the frequency of clock can be half of the clock frequency in single edge triggered logic.

Low-Swing clock Double-edge triggered Flip-Flop (LSDFF) has been developed to reduce power consumption compared to conventional flip-flop [10]. Power consumption in clock tree is reduced, using low swing clock and low-Vt transistors in FF. subthreshold current of low-Vt transistors in FF. subthreshold current of low-Vt transistors in main logic is controlled by high-Vt transistors but the subthreshold current of low-Vt transistors in inverters that is used in clock tree incur more power consumption in clock tree especially in very deep submicron technology. Furthermore, number of transistor in this logic is much greater than previous works.

In this paper a Modified version of HLFF (MHLFF) is proposed that has lower number of transistors as well as less power consumption and delay compared to HLFF. Then, by applying additional modification to this logic, a new logic called Double-edge triggered Modified Hybrid Latch Flip-Flop (DMHLFF) is developed. In this new logic, reduction of power consumption in clock tree is achieved by decreasing the frequency of clock to half of the frequency of HLFF and SDFF in same application.

This modification let DMHLFF to be comparable to LSDFF in the case of power consumption. However, DMHLFF is much faster than LSDFF. This paper is organized as follows. In Section 2, the structure of FFs explained and compared with each other. The development of DMHLFF is described in section 3. Section 4 discusses the simulation results. The paper ends with conclusions in Section 5.

2. REVIEW OF FLIP-FLOP STRUCTURES

The structure of Hybrid Latch Flip-flop (HLFF) is shown in Figure 1 [6]. HLFF has very simple structure but the unnecessary internal transition increase the total power consumption of flip-flop. Every time, the input is high a glitch is generated, regardless of previous state of the output [3]. Furthermore, the transistors in stack degrade the performance of the logic. These disadvantages make HLFF not suitable for application where low power is required since its power consumption limits its utilization.

In Figure 2 [7] the circuit diagram of Semi-Dynamic Flip-Flop (SDFF) is illustrated. This logic is faster than HLFF due to lower number of transistor in stack, but, the total number of transistor is greater than HLFF. Similar to HLFF, unnecessary internal node transition exists in SDFF. Let’s explain the drawback of SDFF. Suppose that input has high logic value in two successive clocks. Node Q has high logic value and node $X$ is pre-charged to $V_{dd}$ when clock is low. At rising edge of clock, there is a short circuit path from Q to gnd until the node $X$ is discharged. Hence 1-1 glitch exists that causes more power consumption.
To avoid unnecessary transition in previous logic, we propose a Modified Hybrid Latch Flip-Flop (MHLFF) shown in Figure 3. Compared to HLFF and SDFF, the internal node transition in MHLFF occurs only when input has different logic value in two successive clocks. Signal $CLK$ is shifted in time (i.e. equal to delay of inverters chain) to generate $CLKBD$. $C1$ will be high at rising edge of clock and stay high for a period determined by the inverter chain (Figure 4). Depending on the state of input, node $X$ is charged to $V_{dd}$ or remains at low state. Suppose that $D$ has high logic value. At rising edge of clock, node $X$ is discharged through $MN1$ and $MN3$ hence $Q$ is charged to $V_{dd}$ and remains high during the clock period. Hence $MP1$ will be off. If $D$ has high value in the next rising edge of clock, in contrary to previous logic, there is no transition in $X$, thus the extra power consumption is avoided. Compared to HLFF, the state of flip-flop is used to keep the state of internal node until input condition is changed. $MP1$ is a small pull up device, to have little fighting during input state changing in successive clocks. The number of transistors in stack in this structure is less than that in HLFF, so the MHLFF is faster than HLFF.

3. DOUBLE-EDGE TRIGGERED MHLFF

The circuit diagram of Low Swing clock Double edge Flip-Flop (LSDFF) is depicted in Figure 5 [10]. The input of flip-flop is transferred to the output at rising and falling edge of clock. To reduce the power consumption of clock tree, the low swing clock is used in this logic. To have proper operation some of high-$V_t$ transistors are replaced with low-$V_t$ transistors. The subthreshold current of these transistors is controlled by high-$V_t$ transistors in logic. For the same application and operational speed, the frequency of clock in LSDFF could be half of frequency of clock in HLFF or SDFF. Using the low-$V_t$ in stack, cause greater delay in transferring input to the output compared to previous logic.

The power consumption of clock tree is proportional to clock load, frequency and the swing of clock. Compared to previous logic, the swing and frequency of clock is lower. So the power consumption of LSDFF clock tree could be very low than others. However, uncontrolled subthreshold current in clock tree due to using low-$V_t$ transistors, incur extra power consumption. To have this property (Double edge), a new logic, called Double edge triggered Modified Half Latch Flip-Flop (DMHLFF), is proposed. For developing DMHLFF only three transistors (MN5, MP4, and MN6) is added to MHLFF structure as seen in Figure 6. The operation of DMHLFF is similar to HLFF except in falling edge of clock.
At falling edge of clock, C2 is high and input is transferred to output (Figure 7). MN6 is a small transistor, which forces MN5 to be off when CLKBD has high logic value. These properties (low area and double edge) make this logic very interesting in application such as in testing where time of test and area overhead of test circuit is so important. Avoiding unnecessary internal node transition reduces the power consumption in scan chain without any area overhead compared to HLFF and SDFF. Simulation results in the next section confirm that DMHLFF has better performance than previous logics. The waveform of C1, C2, and the output using HSPICE is depicted in Figure 8.

4. SIMULATION RESULTS

Comparison between SDFF, HLFF and MHLFF is shown in Table 1. HSPICE with 0.18-µm CMOS process has been used for simulation. The simulation conditions were 2V $V_{dd}$ with the frequency of clock at 100 MHz and the load of FF is supposed to be 0.05 pF. As seen in the table, the lower power consumption of MHLFF with improvement in delay and area compare to others makes this logic so interesting.

Table 2 illustrates the comparison results of LSDFF and DMHLFF. The frequency of simulation was 50 MHz while voltages of the low swing clock and power supply are 1.5V and 2V respectively. Column 5 in table shows the power consumption of clock tree and column 6 illustrates the total power consumption of the logic (main logic and clock tree). The last column illustrates the power-delay product of corresponding structure. The table shows the difference between power consumption of clock trees and indicates subthreshold currents of low-$V_t$
transistors incur more power consumption. It is obvious that DMHLFF has better performance than LSDFF. The lower number of transistor is the main advantages of DMHLFF than LSDFF in application such BIST where area is so important. The power consumption of clock tree in LSDFF is lower than DMHLFF. However, total power consumption in DMHLFF is less than LSDFF due to the fewer number of transistors and internal node transition in DMHLFF compared to LSDFF. Power consumption of a circuit depends strongly on its structure and the statistics of the applied data. Thus, power measurements should be conducted for the range of different data patterns [11]. Figure 9, depicts the power consumption of various structures for different data pattern. DMHLFF has least power consumption especially when the input pattern does not change.

Table 2: Comparison between LSDFF and DMHLFF structures

<table>
<thead>
<tr>
<th></th>
<th>No. of Tr.</th>
<th>No. of Clked Tr.</th>
<th>D-Q (ps)</th>
<th>Power Of clk tree(uW)</th>
<th>Total Power (uW)</th>
<th>P.D (fJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSDFF</td>
<td>28</td>
<td>3</td>
<td>210</td>
<td>9.5</td>
<td>42.3</td>
<td>8.8</td>
</tr>
<tr>
<td>DMHLFF</td>
<td>20</td>
<td>3</td>
<td>180</td>
<td>14.7</td>
<td>39</td>
<td>7</td>
</tr>
<tr>
<td>changes</td>
<td>-29%</td>
<td>0%</td>
<td>-14%</td>
<td>-35%</td>
<td>-7%</td>
<td>21%</td>
</tr>
</tbody>
</table>

Simulation result shows that the power-delay product of DMHLFF is 47% better than SDFF. These improvements are 39% and 21% compared to HLFF and LSDFF respectively. Improvement can be presented as $\text{Improvement} = ((1 - \text{P.D of the DMHLFF} / \text{P.D of structure}) \times 100 \%)$.

Similar to previous logic DMHLFF can embed the basic element such as NAND, OR … etc gates. The embedded structure is faster than discrete structure as has been shown in previous works [10].

5. SUMMARY AND CONCLUSION

A new Double edge triggered Modified Hybrid Latch Flip-flop (DMHLFF) is proposed that has better performance compared to previous logic. The unnecessary internal node transition is avoided in this logic. Capability of this logic to work with low clock frequency compared to single edge triggered FF leads to low power consumption. Furthermore reducing the number of transistor in stack, decrease the delay of the logic compared to previous works. Simulation results indicate that compared to other structure the performance of DMHLFF is approximately between 21% and 49% compared to previous works.

Figure 9: Flip-flop power consumption dependent on data patterns

REFERENCES