A Low Input Voltage DC-DC Converter with Zero Current Detection Circuit and Delay-Based Timing Control for Thermoelectric Energy Harvesting

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Abstract— This paper presents a new zero current detection (ZCD) circuit with no static power consumption. Proposed ZCD can be used in low input voltage boost converters such as thermoelectric energy harvesters. Also a delay-based timing system has been proposed. Introduced timing circuit can build independent on/off times which enables different frequency and duty cycle variations. This enables lower switching frequency at light loads and improves efficiency. Proposed system has been designed and simulated in 0.18μm CMOS technology and achieves maximum efficiency of 63%.

I. INTRODUCTION

Rapid advances in IC design technology have decreased feature size and power consumption of electronic devices. Small size and low power electronics enable realization of implantable biomedical devices. For implantable devices battery replacement may be difficult or even impossible. There are different energy sources such as vibration, thermoelectric generators (TEG), electromagnetic waves, and piezoelectric conversion that can be used as virtually indefinite energy sources for implantable devices.

All above mentioned energy sources need an extra power management system in order to deliver a regulated power supply. For example a TEG generates a very low voltage related to the temperature difference between its two sides [1]. For biomedical applications, while one side is placed under the body skin which has an almost constant temperature, the other side is subject to different ambient temperatures. So a DC-DC converter that can step up very low input voltages over a wide range of loads is needed to power up the following circuits.

There are many challenges in designing a DC-DC converter for harvesting energy from TEG. The converter’s controller should be designed to dissipate as low power as possible, at the same time having acceptable load regulation. Previous studies on DC-DC converters include designs for harvesting energy from different sources such as thermoelectric, RF and vibration. One of the most challenging issues in designing a DC-DC converter is zero current detection (ZCD) for appropriate switching timing [2,3]. One method is to use a comparator for ZCD. This method is called reactive gate switching [4,5]. This method requires a very fast comparator which consumes power and has offset problems. In [6] a digital control has been used to find the correct switching time. The proposed method is very efficient at the cost of design complexity. It also needs high frequency clock system that consumes power. In [2] a ZCD circuit has been proposed which consumes static power.

This paper presents a simple and effective ZCD circuit with no static power consumption. The effectiveness of the proposed method is validated through simulations. Also a clock free digitally controlled timing system has been introduced. The paper is organized as follows. Section II presents ZCD and timing circuits. In Section III design methodology has been illustrated. Effectiveness of the proposed system has been validated through simulations in Section IV. Conclusions are given in section V.

II. PROPOSED ZCD CIRCUIT AND DIGITALLY CONTROLLED ON/OFF TIMING

Fig. 1(a) shows a circuit implementation of synchronized boost converter. These converters can be used in two different modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The main difference between them is that in DCM the inductor current is prevented from flowing in the reverse direction. As shown in [7] the DCM is more efficient when the average input current is less than half the ripple current. As mentioned in the previous section the key point is synchronizing the P-MOS switch with the moment that inductor current falls to zero. A ZCD circuit can be used for this purpose. Also, using pulse-frequency modulation (PFM), efficiency can be improved on light loads [7]. Therefore using low frequencies at light loads can increase efficiency since switching loss decreases at lower frequencies. Fig. 1(b) shows identical waveforms of an ideal DCM boost converter. Since in steady state average voltage across inductor is equal to zero, boost converter’s
conversion gain can be obtained as:

\[
\frac{V_{OUT}}{V_{TEG}} = 1 + \frac{T_N}{T_P}
\]  

(1)

Since the inductor current is continuous at \( t=T_N \), the voltage at node \( V_D \) goes high (because after \( M_N \) turns off \( V_D \) node becomes high impedance) and turns on \( M_1 \) forcing \( V_{GMP} \) to go low and which turns on \( M_P \). Fig. 2(b) shows equivalent circuit when \( M_P \) is turned on. Having initial inductor current and considering output capacitor to be very large, the inductor current can be obtained as:

\[
i_L(t) = \frac{V_{TEG} T_N}{L}
\]  

(2)

Voltage at node \( V_D \) can also be obtained as:

\[
V_D = V_{OUT} + R_{ON} i_L
\]

(3)

As inductor current reaches zero the voltage at node \( V_D \) reaches \( V_{OUT} \). Negative current in inductor causes \( V_D \) to go lower than \( V_{OUT} \). Once \( V_D < V_{OUT} \), \( M_1 \) is turned off and when \( V_D < V_{OUT} - V_{THP} \), \( M_2 \) is turned on. This forces \( V_{GMP} \) to go high and \( M_P \) is turned on. Choosing low threshold voltage for \( M_1 \) and high threshold voltage for \( M_2 \) can reduce the time needed for \( M_1 \) to turn off and \( M_2 \) to turn on which leads to proper zero current switching. Fig. 2(c) shows identical waveforms using proposed ZCD. Considering zero inductor current switching, which means neglecting the time taken for \( M_1 \) to turn off and \( M_2 \) to turn on, \( M_P \) on time \( (T_P) \) is obtained as:

\[
T_P = L \ln \left( \frac{i_{L0} R_{ON}}{V_{OUT} - V_{TEG}} \right)
\]  

(4)

Considering (5), as \( T_N \) increases, \( T_P \) also increases but with a lower rate which makes conversion gain to increase and vice versa. So \( T_N \) can be used to control conversion gain.

**A. Proposed ZCD circuit**

Fig. 2(a) illustrates circuit implementation of the proposed ZCD circuit. Inductor current after \( M_N \) switch turns off \( (t=T_N) \) can be expressed as:

\[
i_L(t) = \frac{V_{GMP} T_N}{L}
\]

Fig. 2(a) illustrates the overall block diagram of the proposed timing system. When one delay element is working the other one is in standby mode consuming no power. On time is produced with one delay element and off time is produced with the other one. Each delay element is controlled with a digital 4-bit delay control signal. As it can be seen in Fig. 3(b), both on time and off time can be controlled independently which enables wide range frequency and duty cycle variations. On time can be used to control N-MOS switch in Fig. 2(a) for a desired conversion gain and off time can be selected due to load variation.

**B. Digitally controlled on off timing**

All DC-DC converters need timing signals in order to control switches. It is very popular to build a high frequency clock and use frequency dividers to make desired timing signals as in [6,8]. This method consumes power because of high frequency clock system and also needs complex digital circuits. The proposed method decreases power dissipation because it decreases overall circuit activity at light loads.
fast rise time. The selected load capacitance is discharged through \( M_{N1} \) as a switch and \( M_{N2} \) as a current source. The inverters convert the output voltage to digital levels.

C. Circuit Elements Design

Since N-MOS and P-MOS switches affect efficiency, they need an optimal design. As their width increases, channel resistance decreases and improves efficiency while at the same time driving losses increase which degrades efficiency. P-MOS size also affects proposed ZCD delay time so it has been chosen smaller. After many simulations N-MOS and P-MOS widths were adjusted to 1.0mm and 0.1mm respectively.

An off-chip 4.7 \( \mu \)H inductor and a 10nF off-chip capacitor as in [6] were selected that well satisfies appropriate constrains on resistive losses, switching losses, ripple, and area.

IV. SIMULATION RESULTS

The circuit was simulated in a 0.18\( \mu \)m mixed-signal CMOS models using HSPICE. Normal threshold voltage in this technology is 0.45V. TEG was modeled as a DC source. Output capacitance was precharged to 1V as startup. Control bits were set manually to have a 1V output voltage at the lowest possible frequency. A resistive load was also used.

Converter’s efficiency is calculated over a variety of input voltages in different loads. Converter’s performance is summarized in Table I. In case I normal \( V_{th} \) transistors have been used and in case II low \( V_{th} \) for \( M_{1} \) and high \( V_{th} \) for \( M_{2} \) have been used. Low and high \( V_{th} \) devices were simulated by adding external 0.3V DC sources. Simulations show in case II efficiency can be improved up to 10%. Case II is more efficient in very low input voltages compared with case I. This may happen because input voltage \( (V_{TEG}) \) is added to voltage at node \( V_{GD} \), that improves \( M_{1} \) and \( M_{2} \) switching and reduces effect of modified \( V_{th} \) devices. Since output voltages are not exactly the same in all cases, delay elements produce different delay times with the same input codes. This causes small differences in \( T_{D} \). Switching frequency reduction improves efficiency at light loads. Lower reported efficiency at higher input voltages (75mV and 100mV) and light loads is due to off time delay element limitations that is unable produce greater delay times. To improve efficiency in these cases, timing system can be switched on and off based on a signal that detects output voltage.

Fig. 4 shows output voltage ripple and voltage at node \( V_{D} \) for a 20mV input and a 10\( \mu \)W load. Fig. 5 illustrates inductor current and \( V_{GAMP} \). As shown in Fig. 5 \( V_{GAMP} \) goes high slightly after the inductor current has passed zero. Using low \( V_{th} \) MOS for \( M_{2} \) and high \( V_{th} \) MOS for \( M_{1} \) can improve performance. As shown in Fig. 5 using modified \( V_{th} \) devices, \( V_{GAMP} \) goes high just as the inductor current passes zero.

Fig. 6 compares simulated efficiency with those reported in [6]. It has to be noted that in [6] control circuit has also been included and its power consumption has been considered, while in proposed converter, control circuit power consumption has not been included. As shown in Fig. 6, proposed method shows better performance in very low input voltage. Especially in case II, simulated efficiency in 1\( \mu \)W.
and 10µW load is significantly greater than [6]. Higher efficiency in 1µW load can be due to not considering control circuit power consumption. But in 10µW load, higher efficiency can be due to lower switching frequency and using proposed ZCD that consumes no static power.

**Fig. 4.** Simulated output voltage ripple. (b) Voltage at node VD.

**Fig. 5.** (a) Simulated inductor current. Voltage at node (b) VGMP and (c) VD.

**TABLE I. SIMULATED CONVERTER'S PERFORMANCE**

<table>
<thead>
<tr>
<th>Input Voltage (mV)</th>
<th>Load (µW)</th>
<th>( T_s ) (ns)</th>
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**Fig. 6.** Efficiency comparison between this work (case I and II) and [6] for VTEG=20mV VOUT=1V with different loads.

*A Control circuit power consumption has also been considered.

**V. CONCLUSION**

A new ZCD circuit was introduced. Proposed ZCD circuit was used in an ultra low voltage boost converter and its functionality was validated. Also a delay-based timing system was proposed that controls on and off times independently. Overall system was designed and simulated. The system is able to step up input voltages as low as 20mV and can provide output power up 10µW over a precharged output capacitor. Converter’s Maximum achieved efficiency is 63% using modified \( V_{th} \) devices. Dynamic biases can be used instead of using modified \( V_{th} \) devices in order to further improve efficiency.

**References**


