THE IMPACT OF SOLID STATE FAULT CURRENT LIMITER ON COORDINATION BETWEEN PROTECTIVE DEVICES OF DISTRIBUTION GRID IN THE PRESENCE OF DISPERSED GENERATIONS

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Abstract: Distributed generation (DG) is predicted to play an increasing role in the electric power system of the near future. DGs are being introduced to power systems to secure the electric power supply. However, expose of DG, can alter the fault current during a grid disturbance and disturb the existing distribution protection system. After connecting DG, part of the system may no longer be radial, which means the coordination might not be hold. This will give rise to fault current which is normally greater than interrupt capability of reclosers and fuses. The degree of the problem tends to increase when several DG sources are installed in the system. The introduction of Solid State Fault Current Limiters (SSFCLs) becomes an effective way for suppressing such a high short-circuit current fault in distribution systems. In this paper a solid state fault current limiter (SSFCL) application is proposed to minimize the effect of the DG on the distribution protection system in a radial system during a fault. Simulation is accomplished in PSCAD/EMTDC.

Keywords: Solid state fault current limiter, Distribution system, Distributed generation, Recloser-fuse coordination.

1. Introduction

Rising public awareness for environmental protection, increasing energy consumption, lack of power generation, steady growth in power deregulation and utility restructuring lead to increasing usage of Distributed Generation (DG) systems. DG systems installed near load centers due to tight constraints imposed on the construction of new transmission lines for long-power transmission [1, 2]. Distributed Generation (DG) is currently attracting both distribution utilities and electricity users. DG can provide meaningful advantages for not only its owner, but also the utility to which it is connected. The advantages of DG are of both engineering and economic view points. The advantageous applications of DG can be summarized as follows: backup generation, loss reduction, power quality improvement, grid expansion postponement, environmental concerns, peak load service, rural and remote application, combined heat and power generation, and financial and trading purposes [3-5]. Beside the benefits which can be gained by DG, the integration of DG into existing networks brings up several technical, economical and regulatory questions. In terms of physical integration, protection is one of the major issues [2]. By introducing DG to distribution network, due to increasing the fault current, the circuit breakers, protection relays, reclosers and fuses designed for a normal distribution network are affected and may not operate properly [6, 7]. More addition, distribution protection system includes many devices that must be coordinated with each other to operate and eliminate short circuit current properly. This can be achieved by short circuit calculations during system design. Installing DG increases fault current. Thus, some of the protection devices need their setting renewed [2, 4]. As a result of increasing Electricity demand, the distribution systems are continuously expanding. This expansion may result in higher fault current levels at some points of the distribution system. This can be clearly observed when introducing new DG such as wind farms in remote areas. With DG fault current at some points in the network may increased beyond the rating of the existing switchgears. This may demand upgrading of the switchgears with higher short circuit ratings. However, upgrading the switchgears may not practicable due to: (a) high initial cost; and (b) reduction of system reliability during the
construction period. These problems can be overcome by limiting the fault current to an acceptable level. In order to limit the fault current, it is possible to use several techniques such as network splitting, current limiting reactors, sequential network tripping schemes and fault current limiters [8], [9]. It was recognized that Fault Current Limiter (FCL) is a good competitor for limiting the fault current [9]. Employing FCLs is a new solution to limit the fault current produced by DG. The implementation of FCLs in utility system helps to decrease fault current level and prevent changing the circuit breakers and fuses [2], [10], [11].

Different configurations of fault current limiters are proposed to mitigate the impact of DG on distribution protection system [11, 12]. The implementation of FCLs in electric power systems is not restricted to suppress the amplitudes of the short circuits; they are also applied in variety of performances such as the power system transient stability enhancement, power quality improvement, reliability improvement, increasing transfer capacity of system equipments and inrush current limitation in transformers [12].

In this paper a solid state FCL is used to minimize the impact of DG on fault current levels and distribution protection system. The Solid State Fault Current Limiters offer a superior solution to the power distribution system problems caused by high available fault current [13]. A solid state fault current limiter can limit a fault current passing through it within one half cycles [13].

Solid state fault current limiters (SSFCLs) are expected to bring considerable technical and economical benefits to electric power systems such as: limited fault current, limited inrush current (soft start), even for capacitive loads, repeated operations with high reliability and without wear-out, reduced switching surges and improved power quality for unfaulted lines [13]. The feasibility of different concepts of SSFCL has been widely demonstrated during the last decades by means of several laboratory scale prototypes. Some SSFCL prototypes have already installed have been successfully submitted to long term field test [13]. However the choice of the most suitable type of SFCL is not a trivial task since it involves many technical and economical aspects including effectiveness of its limiting effect, losses, interruption capability, interruption time, running costs and size and moreover it is strictly related to the position within the network and therefore to the voltage level and the existing protection scheme and apparatus [14].

In this paper, after review of configuration, operation and activation timing of proposed solid state FCL, we consider the SSFCL effect on reduction of DG produced fault current, in order to restore recloser and fuse coordination and fuse interruption capability.

2. Solid State Fault Current Limiter

Recent developments in power switching technology have made solid state limiters suitable for voltage and power levels necessary for distribution system applications. At present paper, solid state FCL (SSFCL) which is designed in [28-16] is used and its effect on fault current in distribution system in presence of DGs is investigated.

2.1. Configuration of Solid State Fault Current Limiter

This model is based on IGCT power electronic switches. The most beneficial property of this configuration is simplicity of structure and control, low steady-state impedance, fast response and high impedance fault. Fig. 1 shows the topology of the single phase SSFCL as proposed [15].

![Fig.1 Basic configuration of solid state FCL](image1)

The model consists of the DC reactor (L1), Two diodes, Two self turn-off IGCT, Current limiting by-pass reactor (L2) and Zinc oxide surge arrester to prevent over-voltage across the FCL. By optimizing the size of the inductors and with the introduction of switches that can handle high power, this type of FCL can be made relatively compact in size. The authors in [16] provide a good overview of the technical details involved in the model.

2.2. Operation Principle and Sequence Events

In steady-state proposed solid state FCL has not any impact on normal operation of the network. But when a fault occurs, they must insert determined impedance to the network, in order to reduce the fault current. Solid-state types of limiters harness the capabilities of power electronic switches fast operation. Hence they are able to commutate current in the order of a few milliseconds while withstanding high breakdown voltage. Consider Fig.2 that is reproduced from Fig.1. The basic operation principle is as follows:

1. For time \(t < T_{\text{fault}}\), the IGCT T1 and T2 and the diodes D1 and D2 remain in full conduction. All current flows through the diode-IGCT bridge (Path A) with one pair of diode and IGCT switched during the positive cycle and the other pair during the negative cycle. The current through L1 is constant and the voltage drop across L1 is zero.

2. At time \(t = T_{\text{fault}}\), a bolted three phase-to-ground fault is inserted right at the terminals of solid state FCL on the load side.
3. At time \( t = T_{\text{fault}} + \text{Time Delay1} \) (TD1, optional), the fault existence is detected by solid state FCL.
4. At time \( t = T_{\text{fault}} + \text{Time Delay1} \) (TD1, optional) + Time Delay2 (optional), T1 and T2 are gated OFF and all the current is now commutated through the bypass reactor L2 and the current now flows through “Path B”. Also, some of the remaining current freewheels through the diodes D1, D2 and inductor L1, until it falls to 0.
5. For \( t \geq T_{\text{fault}} + \text{fault duration} \), the fault is kept inserted in the system.
6. At time \( t = T_{\text{faultclear}} \), the fault is removed.
7. At time \( t = T_{\text{faultclear}} + \text{Time Delay3} \) (TD3, optional), the IGCT T1 and T2 are gated ON to resume steady state current flow as per “Path A”.

2.3. FCL Activation Timing
Timing the operation of FCL triggering is of paramount importance when modeling any device. The time of activation of a FCL can be a function of its physical properties or user settable parameters via a relay or built-in timers. Fig. 3 shows the FCL activation timing diagram.

![FCL Activation Timing Diagram](image)

Fig. 3 Solid-state FCL activation timing diagram. TD-1/2/3 Time Delay (ms) (optional)


From Fig. 3, a fault is inserted at time 1. Immediately, the magnitude of the line current increases and the “Magnitude flag” is raised. Also, the “Rate of change flag” is asserted since the rate at which line current changes is non-zero. After waiting for a few milliseconds (optional), Turn-off signal is sent to thyristors. This procedure is applicable to most of the kinds of FCL.

Typically in industrial automation and control, a time delay (TD) is added before any action is taken. This is especially true if the action to be taken is dependent on input from sensors, limit switches, proximity switches, etc. by doing so, momentary switching which would otherwise trigger an action is eliminated. Similar concept can also be applied to a power protection. Many times, faults come and go at an instant. This might happen because of a tree touching the line due to windy weather or squirrel trying to jump between lines or even momentary in-rush currents due to a heavy load coming online. Hence, the goal would be to trigger the FCL only after making sure that there is indeed a fault. This is possible by inserting a delay timer. Appropriate delay times can be 2 to 3 cycles or more. A similar delay timer can be used when switching off the FCL. This is done by making sure that the fault has been cleared before turn-off signal is sent to thyristors [16].

3. Installing Solid state FCL in Series with DG
As shown in Fig. 4, a real distribution network with 2DGs is considered. This network is a part of distribution system, the DGs inject fault current to the network and therefore, the level of fault current in the network increases. This may leads to fault current that will be greater than recloser and fuses interrupt capability or may be cause miss coordination between fuses and recloser. For reduction of the fault current, the SSFCL is used in series with distribution system. In this case during the fault, the SSFCL insert series impedance into the network and minimizes the effect of DG on increasing fault current.

4. Simulation
The effect of the SSFCL on a test system (Fig. 4) will be determined by its impact on the 3 phase short circuit current during the fault. PSCAD/EMTDC software package is used to simulate the proposed network. The DGs are modeled by synchronous machines. The simulation parameters are chosen as follow,

Table 1 (a) Distribution System parameters (b) System Load parameters

(a) Active\(\text{W}\) Reactive\(\text{kVAR}\)
| L1 | 0 | 0 |
| L2 | 810 | 460 |
| L3 | 628 | 470 |
| L4 | 612 | 791 |
| L5 | 616 | 378 |
| L6 | 474 | 344 |
| L7 | 1342 | 1078 |
| L8 | 920 | 292 |
| L9 | 766 | 498 |
| L10 | 662 | 480 |
| L11 | 896 | 198 |
| L12 | 1292 | 554 |
| L13 | 1124 | 480 |

(b)\(\text{P}(\text{kw})\) \(\text{Q}(\text{kvar})\)
| 1 | 2 | 0.176 | 0.138 |
| 2 | 3 | 0.176 | 0.138 |
| 3 | 4 | 0.045 | 0.035 |
| 4 | 5 | 0.069 | 0.069 |
| 5 | 6 | 0.045 | 0.035 |
| 6 | 7 | 0.116 | 0.081 |
| 7 | 8 | 0.073 | 0.073 |
| 8 | 9 | 0.074 | 0.058 |
| 9 | 10 | 0.093 | 0.093 |
| 10 | 11 | 0.063 | 0.05 |
| 11 | 12 | 0.098 | 0.093 |
| 12 | 13 | 0.062 | 0.093 |

Assume before connecting DG, a three-phase fault occurs in bus13 at \( t = 1 \) sec and last for 5 cycles (100ms). Fig. 5(a) and (b) shows the fault and recloser current
waveform and RMS. This fault current, \( I_{(\text{old})} \), equals to 9.17kA. Tabulation of fault duty for recloser and fuses is shown in Fig. 5(c). It has been clear that \( I_{(\text{old})} \) is between \( I_{\text{k,min}} \) and \( I_{\text{k,max}} \). So, recloser at fast mode can operate faster than fuse13 and fuse13 can also operate faster than recloser at slow mode. Therefore, protection coordination between fuse13 and recloser exists and fuse has the capability of current interruption.

Fig.4 real 13 bus distribution network

To investigate the effect of integrating DGs in the proposed network, two DGs are installed at bus 9 and bus 11 and three-phase fault occurs in bus13 at \( t=1 \) sec and last for 5 cycles (100ms). Fig. 6(a) and (b) shows the fault, \( I_{(\text{new})} \), and recloser current waveform and RMS in presence of DGs. According to Fig. 5 and Fig. 6, in presence of DGs the fault current level increases. As shown in Fig. 6(c), \( I_{(\text{new})} \) is greater than interrupt Capability of fuse8 then fuse8 must be replaced, because it doesn't operate during the fault properly. Now two solid-state FCL is installed between bus7 and bus11 and between bus8 and bus9. The limiting reactor impedance of this solid-state FCL is about 3.14 ohm. Fig. 7(a) and (b) shows fault current \( (I_{(\text{new})}) \) and recloser current waveform and RMS when a fault occurs in bus13 at \( t=1 \) sec and last for 10 cycles (200ms). As shown in Fig. 7(c), this fault current is decreased and reaches to 13.5kA which is between \( I_{\text{k,min}} \) and \( I_{\text{k,max}} \). So, the solid-state FCL mitigates the short circuit current level. To study the operation of SSFCL, the current and voltage difference across solid state FCL waveform and RMS are shown in Fig.8(a) and (b). It has been clear that limiting reactor enters in the network during the fault and alleviates the short circuit current. Furthermore, in normal operation of the network all current flows through GTO thyristors. Therefore, proposed SSFCL has not any impact on normal operation of the network.

Fig.5 (a) fault, (b) recloser current waveform and RMS without presence of DGs and (c) fuse and recloser coordination

Fig.6 (a) fault and (b) recloser current waveform and RMS in presence of DGs and (c) Fuse and recloser coordination curve and short circuit current in presence of DGs (If (new)).
Fault Current

Presence of DG increases fault current level which may be greater than recloser and fuses interrupt capability or may be cause miss coordination between fuses and recloser. In this paper, in order to reduce the fault current level to desired level inclusion a solid state FCL in distribution system is proposed. The main advantages of the proposed FCL are simplicity of structure and control, low steady-state impedance, fast response and high impedance fault. Also this type of FCL has no effect on utility voltage and current at normal system operation. With computer simulation of a thirteen-bus case study, it was shown that the selection of suitable location and impedance of an FCL could be used to solve problems associated with DG connection. In this paper, the SSFCL is completely simulated, while a fault occurs the SSFCL automatically determined series impedance to the network and after fault clearing the SSFCL automatically removes the impedance from network. The simulation results demonstrate both the ability of proposed FCL to limit the fault current level and minimizing the impact of DG on protection problems. Although this study is based on a particular network the methodology used in this study can be directly applied for the any network.

References


