A Wide Band Envelope Modulator for Envelope Tracking RF Power Amplifiers

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Abstract— polar modulation RF power amplifier is a good candidate to enhance the efficiency while maintaining the linearity for high PAPR signals. Among different architecture used for envelope modulator, hybrid switching envelope modulator is attracted the attention. Class AB power amplifier which is the main block of hybrid switching envelope modulator should have wide bandwidth and low output impedance in a wideband of frequency to compensate high switching noise ripples. In this paper a wideband supply modulator with sufficient low output impedance is designed in 0.18 µm CMOS technology. The bandwidth of the modulator is around 437 MHz which is much larger than previously reported in literature. Thanks to the low output impedance of the class AB architecture, the HSEM architecture is capable of reducing the switching frequency noise up to 100MHz, while consuming approximately the same power as other architecture.

Keywords: CMOS, envelope modulator, power amplifier, current sense, hysteresis comparator.

I. INTRODUCTION

Envelope tracking RF power amplifier (PA) is a popular architecture for enhancing the linearity and efficiency of PAs, for complex modulated signals, like OFDM. As shown in Fig. 1, in this architecture amplitude and phase of the signal are amplified in different paths. Envelope amplifier is the block that is used for modulating the amplitude of the signal at the drain of the main RF power amplifier. Different architectures have been proposed in the literature [2, 4] for implementation of the envelope modulator. Low dropout (LDO) regulator, series/parallel combination of linear and switch mode amplifier are different architectures of envelope modulator.

One of the most popular architectures which have attracted attention is the hybrid switching envelope modulator (HSEM). HSEM as shown in Fig. 2 consists of the parallel combination of class-AB and class D power amplifiers. It provides a desirable combination of wide bandwidth, low ripple and high efficiency. In this architecture class D PA provides the average output current while the linear amplifier mostly used for compensating the switching noise ripple in the true state of the architecture. In order to maintain a high switching frequency the bandwidth of the linear amplifier should be high which results in a higher power consumption of the linear stage. On the other hand the output impedance of class-AB PA should be low in the switching frequency to reduce switching noise ripples. There are some other challenges in the design of the HSEM to obtain a highly linear and efficient architecture.

In this paper behavioral modeling of the HSEM will be discussed. Different challenges that should be considered in the design of HSEM will be investigated by simulation. Class-AB PA designed in [1] will be used in the HSEM model. Simulation results show that the output impedance of class-
AB PA is low enough up to 100 MHz frequency to decrease the switching noise ripples of class D PA. In addition, the bandwidth of the class-AB is high enough to contain switching frequency noise and reduce its effects. The total bandwidth of the HSEM is determined by the bandwidth of class-AB PA and the output filter of class D PA. The HSEM model with designed class-AB has a total bandwidth of 437 MHz which is almost 1.3 times higher than similar architecture with different class-AB PA [3].

The paper is organized as follow. In section 2 behavioral modeling of HSEM will be discussed. After evaluating different challenges of HSEM the class AB PA designed in [1] is used to investigate the performance. Different ideal blocks of the HSEM will be replaced with its transistor level equivalent circuit in the next sections. The overall HSEM architecture performance will be investigated in the last section.

II. BEHAVIORAL MODELING OF HSEM

In this section the behavioral modeling of HSEM shown in Fig. 3 will be explained.

Different challenges and tradeoffs exist in the design of HSEM which has been explained in literature [1, 3, 5-7]. To investigate these challenges of HSEM design and performance of class-AB PA, a model circuit shown in Fig. 3 is used.

As conventional hybrid architecture, Rsense is used to sense the output current of class-AB PA. A differential to single ended configuration with three ideal opamps (OP2-4) is used to convert the differential voltage across Rsense to a single ended one. A conventional hysteresis circuit composed of an opamp and two resistors (OP5, R3 and R4) are used to generate PWM signal for class D PA.

In the first stage, to find the effects of output impedance and slew rate of class-AB PA on the switching noise ripples of output load current an ideal opamp (OP1) is used instead of that. As illustrated in Fig. 4, the output load current ripple is proportional to the output impedance and inversely proportional to the slew rate of class-AB PA. Since the switching frequency noise will be passed through the output impedance of class-AB PA and the load impedance, the lower output impedance will result in lower output current and voltage switching noise.

The class-AB PA designed in [1] is used in the HSEM to investigate its non-ideal effects in the structure performance. The designed class AB is a two-stage architecture with folded cascode as the first stage and class AB output stage as the second one. The characteristics of the designed class-AB PA, in 0.18 μm CMOS process, is summarized in TABLE I. To show the ability of reducing the switching frequency noise of class D PA a one tone 10MHz sinusoidal signal is applied. Fig. 5 shows the simulated class-AB, class D and output load currents. The resultant switching frequency with 90 nH inductor is around 100MHz. As it can be seen from this figure the designed class-AB PA is capable of reducing the switching noise of class D thanks to low output impedance of class-AB PA. The total bandwidth of HSEM depends on the class-AB PA and class D output filter bandwidths. Since the bandwidth of the class D output filter is very high the class-AB PA bandwidth is very important to reduce switching noise. The reason is that the band width of class-AB PA should be high enough to cover switching frequency. So the output current of that can compensate the class D output current switching ripple.
For 10 MHz bandwidth the switching frequency is around 100 MHz. As illustrated in Fig. 5, the bandwidth and output impedance of class-AB PA designed in [1] is sufficient to compensate for output current switching noise up to 100 MHz.

III. SENSE AND CONTROL CIRCUIT

The sense and control circuit is shown in Fig. 7. Isense is coming from the circuit shown in Fig. 6. As shown in the figure, the transistors used for current sensing are scaled by the ratio 25:1 of the class-AB output stage transistors. This scaling is required in order to prevent the current sensing circuit from affecting the class-AB PA characteristics. The selection current will be compared with two threshold current to form a hysteretic architecture and produces a square wave output. This square wave output will be fed to the class D input driver which is used for lowering the delay of the class D PA based on the logical effort theory [8].

The switching frequency of this architecture depends on class D output filter inductor and the thresholds of hysteresis circuit. It should be mentioned that in the hybrid architecture, the switching frequency is independent of the circuit parameters and will be equal to the input signal frequency.

As illustrated in the Fig. 7 the Isense current will be mirrored via M1-M4 transistors to the node A. At this node the Isense current will be compared with Ith1 or Ith1+Ith2 depending on the M10 transistor state which will be turn on during the rising edge of the output voltage of the architecture. So in this architecture the Ith2 determines the hysteresis bandwidth. One of the advantages of this architecture is the elimination of Rsense which is contributed to the power loss.

IV. CLASS D AND DRIVER STAGE

As it was discussed in previous sections in order to reduce the delay, driver stage of class D power amplifier should be designed with the logical effort method. In this paper a conventional class D architecture with one phase driver is used. The size of class D transistors will be optimized to reduce the power loss of this PA. If assumed that the total power loss of class D PA is the sum of the conduction loss and switching loss, it can be written as:

\[ P_d = P_{cond} + P_{sw} \] (1)

Where \( P_{cond} \) and \( P_{sw} \) are conduction loss and switching loss of the class D PA respectively and can be computed with the following equations:

\[ P_{cond} = R_{eq}I^2 = I^2[DR_{omp} + (1 - D)R_{omn}] \] (2)

\[ P_{sw} = C_{eq}fV_d^2 \] (3)

Where \( C_{eq} \) is the output capacitor, I is the average output current and \( R_{omp} \) and \( R_{omn} \) are the switch on resistance of the class D PA output PMOS and NMOS transistors respectively. If a minimum channel length is assumed, the product of \( P_{cond} \) and \( P_{sw} \) is independent of transistor size. So the problem is minimizing the sum of two terms which has the constant product when the only varying parameter is the width of the transistors. The answer is the geometric mean of the two terms i.e.

\[ P_{cond} = P_{sw} = V_{dd}I\sqrt{R_{eq}C_{eq}}. \] (4)

Therefore the minimum loss is

\[ P_{d_{min}} = 2V_{dd}I\sqrt{R_{eq}C_{eq}} \] (5)

After the class D transistors size determined, number of driver stages and stage ratio will be computed based on the

<p>| TABLE I. CHARACTERISTICS OF THE DESIGNED CLASS AB POWER AMPLIFIER IN[1] |
|----------------|----------------|----------------|----------------|</p>
<table>
<thead>
<tr>
<th>Input Stage</th>
<th>DC Gain (dB)</th>
<th>UGBW (MHz)</th>
<th>Output Imp.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>94</td>
<td>702 (with 2pf load)</td>
<td>0.25Ω @ 20 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>470mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SR=600</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SR=1856</td>
</tr>
<tr>
<td>Rail-to-Rail</td>
<td>89</td>
<td>453 (with 2pf load)</td>
<td>0.59Ω @ 125 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>60mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>472mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SR=763</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SR=428</td>
</tr>
</tbody>
</table>

Figure 6. Schematic of current sense circuit

Figure 7. Schematic of hysteresis circuit
ratio of $C_{eq}$ and the output capacitor of the current sense circuit. PMOS transistors size two or three times larger than the NMOS transistors to have the same on state resistance. The output filter of the class D PA determines the bandwidth of the class D PA. The large inductor corresponds to lower switching frequency but at the cost of lower class D bandwidth, higher difficulty for on chip implementation and large signal tracking ability.

V. SIMULATION RESULTS

The frequency response of HSEM architecture is shown in Fig. 8. As illustrated in the figure, the -3dB band width of the total HSEM architecture is around 437 MHz which is approximately 1.3 times higher than the other architecture. As it was shown in Fig. 5 the output impedance of the class AB is low enough to compensate the switching noise ripple up to 100MHz.

![Figure 8. Frequency response of HSEM](image)

Characteristics of the designed HSEM is compared with some of the previously designed HSEM in TABLE II

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Tech. (nm)</th>
<th>Class AB architecture</th>
<th>Class-AB output impedance</th>
<th>Modulator Bandwidth (MHz)</th>
<th>Maximum Switching frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>130</td>
<td>---</td>
<td>---</td>
<td>120</td>
<td>3.75</td>
</tr>
<tr>
<td>[3]</td>
<td>65</td>
<td>3 stage with class-AB output stage</td>
<td>0.42 Ω @ 125 MHz</td>
<td>340 MHz (with 5.3Ω/2pf load)</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>This work</td>
<td>180</td>
<td>2 stage with class-AB output stage</td>
<td>0.59Ω @ 125 MHz 89 μA @ 20 MHz</td>
<td>437</td>
<td>100</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

In this paper a wideband HSEM suitable for polar modulation architecture has been presented. The designed HSEM has a much larger bandwidth while the power dissipation is approximately the same or less than previously reported in literature. This HSEM can be used in a polar architecture for amplifying the high PAPR signal with bandwidth as high as 10 MHz. The low output impedance of the architecture reduces switching frequency noise up to 100MHz.

REFERENCES


