Abstract— In this paper, a reduced-sample-rate 2-2-0 delta-
sigma-pipeline analog-to-digital converter (ADC) is presented. The
proposed architecture offers the possibility of implementing
the reduced-sample-rate structure on higher order modulator
without having stability or digital-to-analog converter (DAC)
linearity problems. By the presented implementation approach
some digital filters are eliminated, saving power at the digital
part of the ADC. Implementing the reduced-sample rate
structure on 2-2-0 MASH delta-sigma ADC with the OSR of 8,
causes the 8-bit pipeline quantizer to work two times lower than
the overall frequency at the expense of 1.5dB losses in SNR, and
this is rewarding in high bandwidth applications. System level
simulation using MATLAB/SIMULINK verifies the usefulness
of the presented structure and 70dB SNR is achieved after the
first decimation.

I. INTRODUCTION

A cascaded delta-sigma-pipeline ADC employs a single-
loop delta-sigma modulator as the first stage and a high-
resolution pipeline ADC as the second stage [1], [2]. In order
to achieve higher order noise shaping and stability of the first
stage simultaneously, multi-bit quantizer and multi-bit DAC
must be used at the first stage [1], [3]-8]. Therefore, dynamic
element matching (DEM) circuitry or adaptive compensation
techniques is needed to overcome DAC non-linearity problem
at the expense of power and area [9-12].

On the other hand, a 2-2-0 MASH delta-sigma-pipeline
modulator is introduced by authors for higher order noise
shaping, having neither stability nor DAC non-linearity
problems [13].

In this paper, a reduced-sample-rate 2-2-0 MASH delta-
sigma-pipeline ADC is presented. In this structure, the
sampling frequency of the pipeline quantizer is N-times lower
than that of the overall modulator, where N is the order of the
decimation filter [14]. Besides, by the presented implementation approach some digital filters are eliminated,
leading to save area and power at the digital part of the ADC.

The rest of the paper is organized as follows: Sec. II
describes a brief background of 2-2-0 MASH delta-sigma-
pipeline modulator. In Sec.III the reduced sample-rate
structure is discussed. Sec.IV presents the proposed ADC
architecture. In Sec.V MATLAB/SIMULINK simulation
results are given and finally the paper is concluded in Sec.VI.

II. 2-2-0 MASH DELTA-SIGMA-PIPELINE MODULATOR

Leslie-Singh structure is introduced in [2] and it has been
developed in [1], [3], [6-8]. This structure is often used in low-
OSR, high-SNR applications. Based on Leslie-Singh
architecture, a 2-2-0 MAH delta-sigma-pipeline modulator is
introduced, taking the advantages of the MASH structure and
the cascaded delta-sigma-pipeline modulators simultaneously
[13]. This architecture offers the possibility of implementing a
fourth-order single-bit quantizer delta-sigma modulator with
the same SNR of a multi-bit quantizer, having neither stability
nor DAC non-linearity problem. The mismatch between
analog and digital component in the pipeline part is also
shaped by the order of two and its deleterious effects are
reduced. The block diagram of the modulator is shown in
Fig.1, and Z-domain equations describing the modulator are
given as following

\[ Y_{out} = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (1) \]

\[ Y_1(z) = STF_1(z)X(z) + NTF_1(z)Q_1(z) \]
\[ = Z^{-2}X(z) + (1 - Z^{-1})^2Q_1(z) \quad (2) \]

\[ Y_2(z) = STF_2(z)Q_1(z) + [NTF_2(z) - H_d(z)]Q_2(z) \]
\[ + H_d(z)Q_3(z) \quad (3) \]

if there are no mismatch :

\[ NTF_2(z) = H_d(z) = (1 - Z^{-1})^2 \]

then \( Y_2(z) \) is as following:

\[ Y_2(z) = STF_2(z)Q_1(z) + H_d(z)Q_3(z) \]
\[ = Z^{-2}Q_1(z) + (1 - Z^{-1})^2Q_3(z) \quad (4) \]

and finally

\[ Y_{out} = Z^{-4}X(z) + (1 - Z^{-1})^4Q_3(z) \quad (5) \]

where \( D \) is the number of the pipeline ADC stages, \( X(z) \) is
the input and \( Y_{out}(z) \) is the output signal of the overall
modulator, \( Y_1(z) \) and \( Y_2(z) \) are the output signal of the first
and second stage modulators, \( STF_1(z) \) and \( STF_2(z) \) are
the signal transfer function of the first and second stage
modulators and \( NTF_1 \) and \( NTF_2(z) \) are the first and second
stage modulators noise transfer functions respectively, \( H_d(z) \)
is a digital filter at the last stage and \( Q_1(z), Q_2(z), Q_3(z) \) are
the first, second and the third stages quantization noises,
respectively. It is clear that the output of the overall
modulator consists of the input signal, \( X(z) \), and just the last
stage quantization noise, \( Q_3(z) \). It is easily understood that the
first and second stage quantization noises, \( Q_1(z), Q_2(z) \) are completely removed from the output signal in the ideal case.

\[
Y_{\text{out}} = Z^{-N}X(z)
\]

By considering the mismatch between digital and analog filter in the pipeline part (\( H_d(z) \) & second stage NTF) and rewriting the output equation, as shown in (6), it is proven that this mismatch is shaped by the order of two and therefore its destructive effect is reduced thanks to this structure.

\[
Y_{\text{out}} = Z^{-N}X(z) + [\text{NTF}_2(z) - H_d(z)]Q_1(z)(1 - Z^{-1})^2 + (1 - Z^{-1})^2 H_d(z)Q_2(z) \quad (6)
\]

It should be mentioned that the sensitivity to digital and analog filters mismatch is also exist in the MASH part because of its MASH nature, limiting the overall SNR.

**III. THE REDUCED-SAMPLE-RATE ARCHITECTURE**

Fig.2(b) shows the block diagram of a delta-sigma-pipeline ADC with reduced-sample-rate architecture, introduced in [14], and the non-reduced-sample-rate structure is shown in Fig.2(a). This structure uses a single loop delta-sigma modulator in the first stage and a multi-bit quantizer in the cascaded stage. Considering the modulator and decimation filter together, the pipeline quantizer can run at lower speed, saving power and area. Using a sinc filter as the first stage for the decimation filter, the transfer function of the Mth-order decimate-by-N sinc filter is

\[
H_{\text{dec}}(z) = \frac{(1 - Z^{-N})^M}{N^M (1 - Z^{-1})^N} \quad (7)
\]

where \( M' > M \). Arranging the first stage NTF as

\[
\text{NTF}_1(z) = H_{d_2}(z) = (1 - Z^{-1})^{M'}
\]

In order to implement the reduced-sample-rate structure \( M \) and \( M' \) must be equal. Thus, as shown in (8) and Fig.2(b), \( H_{d_2}(z) \) cancels the sinc filter’s denominator [15].

\[
Y_{\text{out}(z)}_{\text{decimated}} = X(z) \text{STF}_1(z) H_{\text{dec}}(z) H_{d_1}(z) Z^{-D} + \frac{(1 - Z^{-N})^4}{N^4} Q_2(z) Z^{-D} \quad (8)
\]

where \( H_{\text{dec}}(z) \) is the sinc filter transfer function and \( Y_{\text{out}(z)}_{\text{decimated}} \) is the output of the ADC after the first decimation. Realizing that only \( Z^{-N} \) terms are associated with \( Q_2(z) \), a down-sampled version of \( Q_2(z) \) can be used. The drawback of the reduced-sample-rate structure is that it uses a decimation filter with order of \( M' = M \), and hence it causes a little losses in SNR [4],[13],[14].

**IV. THE PROPOSED ADC ARCHITECTURE**

**A. Architectural considerations**

The reduced-sample-rate structure introduced in [14] cannot realize modulator with non-zero poles stabilizing the loop of the first stage. Thus, some modified techniques are introduced in order to implement ADCs with higher order noise shaping with nonzero poles [3],[16]. But, they have two main problems: first, modified NTF leads to have modified sinc filter, introducing design challenge. Second, because of stability problems in higher order noise shaping, multi-bit internal quantizer and consequently multi-bit feedback DAC must be used. As it mentioned before, using multi-bit feedback DAC, limits achievable performance due to nonlinearity problem. Dynamic element matching (DEM) or adaptive compensation techniques must be used to solve this problem at the expense of power and area [8-10]. In this section, a reduced-sample-rate 2-2-0 delta-sigma-pipeline ADC is presented. This structure offers the possibility of implementation of the reduced-sample-rate structure on forth-order delta-sigma ADC with zero poles and single-bit internal quantizer, which was impossible using conventional structure. The evolution to the proposed reduced-sample-rate ADC with some design considerations in which some digital components are saved, is clearly illustrated in Fig.3. Considering N-fold decimate the output word stream with Mth–order sinc filter, is shown in Fig.3(a). As shown in Fig. 3(b), Fig. 3(c) by some rearrangement, using linear signal properties, multiple of \( H_d(z) \) and \( H_2(z) \), \( [H_d(z) * H_2(z) = (1 - Z^{-1})^4] \), can be cancelled with the denominator of the sinc filter and \( H_2(z) \) can be cancelled with the part of the dominator of the sinc filter, saving area in digital part of the ADC. Therefore, as shown in Fig. 3(d), the multi bit pipeline ADC can be moved behind the down-sampler, thus N times reducing its sample rate. Mathematical description of this evolution is given as:

\[
Y_{\text{out}(z)}_{\text{decimated}} = H_{\text{dec}}(z) * \{ H_1(z)[\text{STF}_1(z)X(z) + \text{NTF}_1(z)Q_1(z)] + H_2(z)[\text{STF}_2(z)Q_1(z) + \text{NTF}_2(z)Q_2(z) - H_d(z)Q_2(z) - H_2(z)Q_3(z)] \}
\]

\[
Y_{\text{out}(z)}_{\text{decimated}} = \frac{(1 - Z^{-N})^4}{N^4} Z^{-D} \left( \frac{1}{(1 - Z^{-1})^4} Z^{-4}X(z) + Q_3(z) \right)
\]
It should be mentioned that because of focusing on low OSR design, low folding ratio such as N=2 is a good candidate for the first stage of the decimation filter [3]. The scaling coefficients are given in Table I. It also must be noted that in Fig.3(a), Fig.3(b) and Fig.3(c) the coefficients are assumed to be one for the sake of simplicity. The final structure consisting of the scaling coefficients is shown in Fig.3(d).

![Fig.3(d). Structure consisting of the scaling coefficients](image)

**TABLE I.** Coefficients of the modulator after scaling.

<table>
<thead>
<tr>
<th>Coefficients</th>
<th>Coefficients</th>
<th>Coefficients</th>
<th>Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_1$</td>
<td>$b_1$</td>
<td>$b'_1$</td>
<td>$b_2$</td>
</tr>
<tr>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
</tr>
<tr>
<td>0.42</td>
<td>0.0525</td>
<td>0.21</td>
<td>1.68</td>
</tr>
</tbody>
</table>

**B. Design consideration and hardware requirements**

Considering 0.1% mismatch for the realization of the analog and digital part of the ADC, it has proven in [13] that the optimum pipeline ADC number of bits for the OSR of 8 is 8-bit. Reduction in the sampling rate of the 8-bit pipeline ADC by the order of N causes saving large amount of power consumption in high bandwidth applications. The hardware comparison of the 2-2-0 structure in [13] and the proposed reduced-sample-rate 2-2-0 in this paper and the conventional 2-2 MASH delta-sigma ADC is given in Table II, assuming same SNR for all the modulators.

One way to increase the SNR in the conventional MASH modulators is using a multi-bit quantizer at the last stage. In order to have same SNR, an 8-bit Flash ADC must be used in the last stage and consequently an 8-bit DAC in the feedback loop. Implementation of an 8-bit Flash quantizer needs 256 comparators and it has severe practical limitations. On the other hand, the 2-2-0 MASH delta-sigma modulator and its reduced sample-rate structure use pipeline quantizer instead, which needs only 15 comparators. In addition, using the multi-bit quantization in the feedback loop strongly affects the performance of the conventional modulator because the employed multi-bit DAC in the feedback loop does not have a good linearity behavior. Thus, digital error matching (DEM) circuitry must be used in order to mitigate the 8-bit DAC non-linearity problem at the cost of the power and area [3], [10]. The hardware requirements of the DEM circuitry increase exponentially by increasing the DAC number of bits and the 8-bit DAC DEM circuitry is strongly power hungry [11]. However, DEM circuitry is not required for 2-2-0 MASH delta-sigma-pipeline ADC and its reduced-sample-rate structure. As mentioned before, by the presented implementation approach some digital filters are eliminated in the reduced sample-rate structure.

**TABLE II.** Comparison of the proposed and conventional MASH ADCs

<table>
<thead>
<tr>
<th>Employed Quantizers</th>
<th>Conventional 2-2 modulator</th>
<th>2-2-0 MASH delta-sigma modulator</th>
<th>Proposed structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>One 1-bit comparator (comp.)</td>
<td>Two 1-bit (2Comp.)</td>
<td>Two 1-bit (2Comp.)</td>
<td>Two 1-bit (2Comp.)</td>
</tr>
<tr>
<td>One 8-bit Flash (256Comp.)</td>
<td>One 8-bit pipeline (15Comp.) Working at fs/N</td>
<td>Working at fs/N</td>
<td></td>
</tr>
</tbody>
</table>

**Table: Employed DACs**

<table>
<thead>
<tr>
<th>Employed DACs</th>
<th>One 8-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEM circuitry</td>
<td>Required for 8-bit DAC</td>
</tr>
<tr>
<td>Others</td>
<td>Severe practical limitation</td>
</tr>
</tbody>
</table>

V. SIMULATION RESULTS

The detailed realization of the proposed ADC architecture is illustrated in Fig.3(d). This architecture and its circuit non-idealities such as finite op-amp gain, gain variation and coefficients mismatch are behaviorally modeled using MATLAB/Simulink [17]. The proposed ADC consists of two second-order single-bit delta-sigma modulator at the first and second stages and an 8-bit pipeline ADC working with the frequency of fs/N (N=2 for this application) at the last stage.

Dynamic range plot of the presented structure compared to non-reduced-sample-rate architecture and single-bit 2-2
MASH is shown in Fig.4. As can be seen, the 1.5dB loss of SNR is the expense of reducing the sample rate of the 8-bit pipeline ADC. Power spectral density function is shown in Fig.5, and 71dB is the maximum SNR which is achieved with -3.6dB sinusoidal input signal.

As shown in Fig.6, assuming 0.1% capacitor mismatch for the realization of the scaling coefficients and by considering 60, 59, 56 and 52dB op-amp dc-gain for the first to fourth integrators respectively, the SNR degradation is 2dB.

VI. CONCLUSION
A reduced-sample-rate 2-2-0 MASH delta-sigma-pipeline ADC is proposed. Using the reduced-sample-rate structure, the pipeline ADC can run N times at a lower frequency than the overall sampling frequency where N is the order of the decimation, saving power and area. The presented structure offers the possibility of implementation of the reduced-sample-rate cascaded delta-sigma-pipeline architecture on fourth-order modulator with the single-bit internal quantizer and zero poles, which was impossible with conventional reduced-sample-rate ADCs. It also can be extended on higher order structures without stability or DAC non-linearity problems. An efficient implementation of the proposed structure is also presented, saving some digital component. System level simulation using MATLAB/SIMULINK is used to verify the usefulness of the presented structure and 71dB SNR is achieved with OSR of 8 loosing less than 1.5dB compared to non-reduced-sample-rate structure.

References