A Fully CMOS Low Voltage Bandgap Reference without Resistors

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Abstract—A new method to generate a reference voltage is introduced. A fraction of the forward voltage of a pn-junction implemented by a PMOS transistor with negative temperature coefficient (TC) is combined with a voltage produced by a CMOS floating proportional to absolute temperature (PTAT) voltage source. The combined output voltage will be a reference voltage with minimum variation with temperature while no resistance has been used in the circuit. The circuit is designed and simulated in a 0.18 μm CMOS technology which simulation results show the circuit is able to generate an output voltage of 695.6 mV with TC of 18 ppm/°C in the temperature range of -20 °C to +120 °C. Monte Carlo analysis considering both mismatch and process variations gives σ/μ=1.08%. The total power consumption of the circuit is about 8.9 μW at the supply voltage of 1.5V.

I. INTRODUCTION

In conventional reference voltage generators the forward voltage of the base-emitter junction of a BJT that has a negative temperature coefficient is combined with a proper factor of a PTAT voltage to get a reference voltage with a near zero TC. In this method the required factor for the positive-TC voltage is usually realized by the ratio of two resistances [1]. This technique gives a fixed voltage around 1.25V. If two voltages with opposite TC first converted to their corresponding currents and after adding to each other the resultant current sent back to a resistor that acts as a current to voltage converter, it will be possible to obtain a bandgap voltage less than 1.25V [2]. But using this method for low power applications involves choosing high resistances to lower the level of currents which leads to occupy a large amount of chip area. In [3] the ratio MOS transistors is employed to create a bandgap voltage reference without using any resistor but the output voltage has minimum temperature coefficient only around 1.25V and so it is not suitable for low voltage applications. In this paper a current with positive temperature coefficient (PTC) provides the bias current of the pn-junction that is realized by the drain/source and n-well regions of a PMOS transistor. The attenuated form of the forward voltage of the pn-junction through a buffer as voltage VN is added to a PTAT voltage VP that is generated by MOS devices working in subthreshold. The combination factors of two components with opposite TC are appropriately chosen to have a near zero temperature coefficient output reference voltage.

II. GENERAL ARCHITECTURE

The block diagram of the proposed circuit is shown in Fig. 1. A positive temperature coefficient current reference (IPTC) provides the bias current of the pn-junction that is realized by the drain/source and n-well regions of a PMOS transistor. The attenuated form of the forward voltage of the pn-junction through a buffer as voltage VN is added to a PTAT voltage VP that is generated by MOS devices working in subthreshold. The combination factors of two components with opposite TC are appropriately chosen to have a near zero temperature coefficient output reference voltage.

III. CIRCUIT DESCRIPTION

The PTC current generator circuit which is used to provide the bias current of the pn-junction has been adopted from [4] by a little modification. In the work presented in [4], NMOS devices that work in subthreshold region are used to create a bandgap voltage reference without using any resistor but the output voltage has minimum temperature coefficient only around 1.25V and so it is not suitable for low voltage applications. In this paper a current with positive temperature coefficient (PTC) provides the bias current of a pn-junction implemented by a PMOS device. A fraction of the pn-junction forward voltage is added to a PTAT voltage generated by MOS devices working in subthreshold region.

In Section II, the general idea behind this work is introduced and the architecture of the proposed voltage reference is reviewed. Section III describes the function of different blocks in the circuit. The complete results of the simulations that have been performed on the circuit are presented in Section IV. Finally Section V concludes the paper.
terminals tied together to solve the body effect problem. Moreover, the channel length of NMOS devices and also that of M5, M9 and M10 are chosen adequately high to minimize the channel length modulation effect.

A. Analysis of PTC current reference Generator template

In Fig. 2 if it is assumed that M3 and M4 operate in subthreshold region their drain current relationship will be:

\[ I_D = I_{S3} e^{\frac{V_{TH}}{V_{PD}} I_{S3}} \]  

where \( I_{S} \equiv \mu V_{th}^2 C_{dep} (1 - \exp(-V_{SD}/V_{th})) (W/L) \) and \( \xi \equiv 1 + C_{dep}/C_{ox} \) with \( C_{dep} \) and \( C_{ox} \) as the MOS depletion and oxide gate capacitance per unit area, respectively. \( V_{th} = kT/q \) is the thermal voltage and \( |V_{TP}| \) is the PMOS threshold voltage. For M3, M4 and M5 we can write:

\[ V_{SG3} = V_{SG4} + V_{SD5} \]  

Using (1), (2) can be written as:

\[ V_{TP} + \xi V_{th} \ln \left( \frac{l_{I3}}{l_{I3}} \right) V_{TP} + \xi V_{th} \ln \left( \frac{l_{I4}}{l_{I4}} \right) + V_{SD5} \]  

Supposing \( \exp(-V_{SD}/V_{th}) \approx 0 \), based on \( I_{S} \) relationship, we have:

\[ V_{SD5} = \xi V_{th} \ln (n) \]  

where \((W/L)_4/(W/L)_5 \equiv n\). Since \( V_{SD5} \) is usually a small voltage, it can be assumed that M5 operates in triode region with the following relationship for its drain current:

\[ I_{D5} = \beta_5 \left( V_{SG5} - \frac{|V_{TP}| - \frac{V_{SD5}}{2}} {} \right) V_{SD5} \]  

where \( \beta_5 = \mu_p C_{ox} (W/L)_5 \), with \( \mu_p \) as the hole carriers mobility. Since M9 with diode connected configuration works in saturation and has the same gate-source voltage as M5, we can write:

\[ V_{SG5} = V_{SG9} = |V_{TP}| + \frac{2I_5}{\beta_9} \]  

By substituting (4) and (6) into (5), we get:

\[ I_1 = \beta_5 \left[ \frac{2I_2}{\beta_9} - \frac{\xi V_{th} \ln (n)}{2} \right] \xi V_{th} \ln (n) \]  

The relationship between \( I_1 \) and \( I_2 \) expressed by (7) is shown in Fig. 3. In the circuit of Fig. 2, M1, M2 and M8 have the same size with equal gate-source voltage so that they have equal drain currents, i.e., we have \( I_1 = I_2 \) therefore the equilibrium points of the circuit will be the intersection of the curve of \( I_1 = f(I_2) \) and the bisector of the first quadrant of the Cartesian plane \( I_1 - I_2 \) which are A and B points as illustrated in Fig. 3. If the circuit places in the operating point of A, because the current level at this point is too small it will be considered as an undesirable operating point and the circuit needs to be moved from this point to the desirable point of B that can be done with the aid of an start-up circuit. Solving (7) for \( I_1 = I_2 = I \), we can obtain the current \( I \) in equilibrium condition:

\[ I = \frac{(2m-1)+2\sqrt{m^2-m}}{2} \beta_5 \xi V_{th} \ln(n)^2 \]  

where \( m \equiv (W/L)_5/(W/L)_9 \). Since \( \mu_p \) in \( \beta_5 \) and \( V_{th} \) change with temperature as \( T^{-1.5} \) and \( T \), respectively, then based on (8), the current \( I \) changes with temperature as \( T^{-0.5} \). Therefore the circuit in Fig. 2 generates a current with a positive temperature coefficient which depends on the process mainly through \( C_{ox} \ln \beta_5 \).
B. Attenuator and Buffer Circuits

The circuit used to make a negative temperature coefficient voltage is shown in Fig. 4(a). The circuit is to be designed in a full digital CMOS technology and thus there is no BJT or ordinary pn-junction accessible to use. As a result a PMOS device has been used to implement the pn-junction in the circuit of Fig. 4(a). The bias current of this junction is provided by the circuit of Fig. 2. Two series diode connected M2 and M3 act as an attenuator which ultimately through a buffer circuit produces a voltage $V_{o}$ as a fraction of $V_D$ with a negative temperature coefficient. The buffer circuit is made by a simple differential pair consisted of M4 to M8 whose output voltage is sent to the next section. In practice, M2 and M3 operate in subthreshold region and since $I_{D2}=I_{D3}$, we have:

$$I_{S2} e^{\frac{V_{SG2}-V_{TP}}{V_{TH}}} = I_{S3} e^{\frac{V_{SG3}-V_{TP}}{V_{TH}}}$$  \hspace{1cm} (9)$$

And thus we have:

$$V_{SG2} = V_{SG3} + \zeta V_{TH} \ln \frac{I_{S3}}{I_{S2}}$$  \hspace{1cm} (10)$$

Because $V_{SG3} = V_D - V_{SG2}$, we can write:

$$V_{SG2} = 0.5V_D + 0.5\zeta V_{TH} \ln M$$  \hspace{1cm} (11)$$

where $M = (W/L)_3/(W/L)_2$. Variation of $V_{SG2}$ with respect to temperature becomes:

$$\frac{\partial V_{SG2}}{\partial T} = 0.5 \frac{\partial V_D}{\partial T} + 0.5\zeta v_{TH} \ln M$$  \hspace{1cm} (12)$$

The first term in (12) is negative with a typical value around $-1$ mV/°C while the second term is positive but its value for typical figures of $\zeta$ and $M$ is usually less than the absolute value of the first term. As a result the TC of $V_{SG2}$ in (11) is negative. The voltage $V_{SG2}$ after passing through a buffer stage is added to a voltage with positive temperature coefficient to get a reference voltage with the least variation with respect to temperature. Fig. 4(b) shows the building block that produces the voltage with positive temperature coefficient. The current level of $I_0$ and the sizing of M10 and M11 are chosen such that both transistors operate in subthreshold. In this condition we can obtain the voltage of $V$ as follows:

$$V = V_{G510} - V_{G511} = \zeta V_{TH} \ln n$$  \hspace{1cm} (13)$$

where $n = (W/L)_{11}/(W/L)_{10}$. The voltage $V$ has a positive temperature coefficient with minimum dependence on process parameters. By using the series connection of three floating PTAT voltage sources we can obtain an appropriate positive-TC voltage. This voltage will be added to the voltage $V_N$ with negative TC The result will be a reference voltage with minimum variation in terms of temperature and process. The final circuit including three stages of the circuit of Fig. 4(b) is depicted in Fig. 5. Transistors Ms1 to Ms4 are used as the start-up circuit.
IV. SIMULATION RESULTS

The reference voltage circuit was designed and simulated by using BSIM4 model in a 0.18 µm CMOS technology. A dc sweep on temperature in the range of −20 ºC to +120 ºC was performed on the circuit while the typical supply voltage was chosen 1.5V. Fig. 6 shows the reference voltage in this condition. The temperature coefficient that is obtained from this figure is less than 18 ppm/ºC. In order to evaluate the effect of process mismatches on the reference voltage, a Monte Carlo analysis with 300 runs considering both mismatch and die to die process variations was performed. Fig. 7 represents the output voltage at the temperature of 27 ºC.

Simulation result gives $\sigma = 7.5$ mV and $\mu = 696.2$ mV that is equivalent to the relative variation of $\sigma/\mu = 1.08\%$. The main reason for the variation of the reference output voltage versus process variations in this circuit is the threshold voltage mismatches between transistors used in the floating PTAT voltage generators. Consequently, choosing large gate area for these devices can significantly reduce the sensitivity of each PTAT floating voltage with respect to the devices mismatches. Having a constant output voltage in spite of supply voltage changes is another important factor in a reference voltage generator design. To minimize the variation of the reference voltage against the supply changes, the cascode structure with long channel length for its devices is used to implement the current source, which provides the bias current of the floating PTAT voltage generators. Fig 8 illustrates the time response of the circuit where a step voltage with 1 ms rise time as the supply voltage has been applied to the circuit. The transient analysis is done in different process corners and extreme points of temperature and supply voltage. The main purpose of this kind of simulation is to make sure that, first, the start up circuit is able to properly run the circuit and secondly, the reference voltage places in an acceptable range at extreme points of the temperature and supply voltage variations.

V. CONCLUSION

A new reference voltage generator without using any resistor was designed. The circuit is appropriate for low power and low voltage applications. By using cascode technique and modified PTC current generator the variation of the output reference voltage is minimized with respect to the power supply voltage variation. In addition to get a stable reference voltage against temperature, process and supply voltage changes, the circuit can provide a rather stable current against the process variation while this current varies with temperature almost as $T^{0.5}$.

REFERENCES


