A Micropower CMOS Analog Circuit for Gaussian Functions

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Abstract: In this paper, a low power CMOS analog circuit that generate the Gaussian function for pattern matching and classification applications is presented. The function is constructed by a novel current mode analog multiplier that is used as a signal squarer and exponential characteristics of MOS transistors in weak inversion. Due to low power consumption, compact structure and wide dynamic range can be easily integrated as a building block of a neural signal processing systems.

Keywords: Neural networks, classification and pattern matching algorithms, Gaussian function, neural hardware, analog circuits, translinear loop in weak inversion

1 Introduction

Pattern matching and classification are applications where neural algorithms show promising capabilities because neural classifier algorithms can easily handle multidimensional problems [1]. In many neural networks, the algorithm for training is based on probability distributions and pattern matches ranked as probabilities of a match [2]. In many cases these probability density functions can be modeled by normal distributions (or combinations).

Although these algorithms primarily implemented in software, but their capabilities to perform many different analog functions such as pattern recognition and image processing make them attractive in hardware implementation. Because of its excellent integration of processing capabilities, the analog approach has been taken in many CMOS neural chips. In this paper a low power analog circuit that produce the Gaussian function for neural or signal processing algorithms is proposed.

Other approaches to implement in CMOS technologies the Gaussian function in weak inversion operation [3,4] or as a piece-wise linear approximation [5] have been reported. The Gaussian function is defined in Equation (1), where \( x \) is the input and \( y \) the output of the

\[
y = Ae^{-\frac{x^2}{2\sigma^2}}
\]

function and \( A, \sigma \) are adjustable constants which define, respectively, the amplitude and the width of Gaussian function.

The function is constructed in three steps. First the input \( x \) is squared by means of a novel topology of a current mode multiplier/divider based on translinear loop with MOS transistors operating in weak inversion region and then converted to proportional voltage with a transistor working in linear region, secondly the voltage level shifted to a proper voltage level and finally an exponential obtained with a MOS transistor operating in weak inversion mode completes the transfer function.

In Section 2 the novel current mode multiplier/divider circuit presented. In section 3 the Gaussian circuit is reported. Sections 4 and 5 present the mismatch effects and simulation results. Finally the conclusion of this brief is presented.
2 Translinear Current Mode MOS Multiplier/Divider

In this section we will use the characteristics of MOS transistor in weak inversion mode. We refer to the following expression of the channel current in a MOS transistor biased in weak inversion [6].

\[ I_D = \frac{W}{L} I_{D0} e^{\frac{v_{DS}}{V_{TH}}} (1 - e^{\frac{v_{DS}}{V_{TH}}}) \] (2)

Where \( W \) is the effective channel width, \( L \) is the effective channel length, \( n \) is exponential slope factor, \( V_{TN} \) is the threshold voltage and \( I_{D0} \) is a current term.

Note on Equation (2) that we can define \( E = 1 - e^{\frac{v_{DS}}{V_{TH}}} \) as a general error term whose value depends on the drain to source value. For \( V_{DS} \) values larger than only 100 mV the value of \( E \) is very close to 1 (\( E > 0.98 \)) then we can assume \( E = 1 \). The error given by this approximation is very low.

Lets take into account the basic translinear loop shown in figure 1. Assuming the same sizes for transistors M1 to M4, ignoring mismatch between devices and using (2), one can find that

\[ I_3 = \frac{I_2 I_4}{I_1} \] (3)

The implementation of the novel current mode translinear multiplier/divider is shown in figure 2. When the current signals input to the circuit, it exploits the translinear principle applied to the loop M1-M4. Transistor M5 sets the potential of source of M2 and set the loop to obtain Equation (3). In this paper we use the circuit as a squarer to multiplying the one of input variable by itself. In this case and using Equation (3), one can find that

\[ I_3 = \frac{I^2}{I_{\sigma}} \] (4)

3 The Gaussian Circuit

The complete circuit is shown in figure 3. M8 works in linear region and is used in strong inversion as a linear resistor. In this region, the drain current can be expressed by

\[ I_D = K.\left[(V_{SG} - V_{TP})V_{SD} - \frac{1}{2}V_{SD}^2\right] \] (5)
Where

$$K = \mu_p C_{ox} \frac{W}{L}$$  \hspace{1cm} (6)

The output resistance of $M_8$ is approximately given by

$$R_{sd,8} \approx \frac{1}{K(V_{DD} - |V_{TP}|)}$$  \hspace{1cm} (7)

Where we assume that $V_{SD,8}$ is small for linear operation

$$V_{D,8} \gg |V_{TP}|$$  \hspace{1cm} (8)

This condition guarantees the operation far from the saturation region and the output current of squarer circuit linearly modifies $V_D,8$ so the drain voltage of $M_8$ is a linear function of the output current of the squarer.

$$\Delta V_{D,8} = -R \frac{I_{x}^2}{I_\sigma}$$  \hspace{1cm} (9)

$M_8$ works in saturated region and acts as a level shifter. $M_8$ shift $V_{D,8}$ to a lower level that is small enough to make $M_{10}$ working in weak inversion to obtain a exponential form to Complete the Gaussian function. We can use Equation (2) and obtain

$$I_{OUT} = I_K e^{\frac{-R I_{x}^2}{n V_\sigma I_{x}}}$$  \hspace{1cm} (10)

Which has the desired Gaussian form given in Equation (1) and $I_K$ is a constant current term, whose value is

$$I_K = I_{D0} \left( \frac{W}{L} \right)_{10} e^{\frac{V_{TN,2}+V_{GS,9}+V_{DD}}{n V_\sigma}}$$  \hspace{1cm} (11)

In fact $I_K$ is the amplitude of the Gaussian function which has a fixed value. To directly control of the amplitude, we can apply the output current $I_{OUT}$ to another multiplier/divider cell that is shown in figure 2 so it could be controlled by a multiplying factor of a reference current. Please note that in Equation (11), the threshold change for $M_8$ due to the body effect represents the percentage variation with respect of the nominal value of $V_{GS,9}$.

In our design, the circuit performs one half of the function. Since the Gaussian function is even function, the other half can be easily implemented by rectifying the input variable.

For specified accuracy of the circuit, the lower limit of variation for $V_{D,8}$ from $V_{DD}$ to satisfy Equation (8) should be calculated. Let us assume an equivalent 8-bit precision over the output current. The upper bound of $\Delta V_{D,8}$ may be calculated by

$$I_{OUT,\min} = I_K \frac{1}{2^n} = I_K e^{\frac{\frac{1}{n V_\sigma} I_{x} R}{I_{x}} V_{D,8}}$$

$$\Rightarrow \Delta V_{D,8} = -n V_\sigma \ln(256)$$  \hspace{1cm} (12)

We obtain, for $\sigma_i = 26 \text{ mV}$, $n = 1$, $|\Delta V_{D,8}| = 144 \text{ mV}$, which is the voltage drop that the output current of the squarer circuit has to generate in order to decrease $I_{OUT}$ to its minimum value $I_{OUT,\min}$

### 4 Limitation of Mismatch

Since the circuit is based on the translinear current mode multiplier/divider, performance is limited by mismatches in the loop $M_1$-$M_4$. Note on Equations (3) and (4) that we assume the case of ideal matching between the devices of the translinear loop, but slightly differences in $I_{D0}$ and $V_{TN}$ of the loop represent a nonlinearity term which affects the circuit operation.

Taking into account these mismatches, the following expression for the output current of squarer $I_3$ can be obtained

$$I_3 = (1 + \Delta I_{D0}) e^{\Delta V_{TN}} \frac{I_{x}^2}{I_\sigma}$$  \hspace{1cm} (13)

Where $\Delta I_{D0}$ is the relative error of $I_{D0}$ in the loop $M_1-M_4$ and $\Delta V_{TN} = V_{TN,2} + V_{TN,4} - V_{TN,1} - V_{TN,3}$. In figure 4, output current relative error for the circuit from figure 2 is shown as a function of $\Delta V_{TN}$ and $\Delta I_{D0}$. It is clear from (10) that the output current of the Gaussian circuit $I_{OUT}$ depends on the error given by Equation (13), through the quantity $\exp(-\frac{R I_{x}}{n V_\sigma})$. 
As a numerical example [7], for a typical process and a NMOS transistor of $W = L = 20 \, \mu m$ we obtain $\Delta V_{TN} = 1.5 \, mV$ and $\Delta I_{D0} = 0.12\%$. As expected, the dominate error is produced by $\Delta V_{TN}$. This explains that $\Delta V_{TN}$ is the main factor of mismatch in transistors working in weak inversion [8]. Even though mismatches cannot be eliminated, they can be kept small enough by means of a suitable layout technique such as common centroid geometry and large transistors, since the mismatch mainly depends on $\frac{1}{\sqrt{WL}}$ [7].

5 Simulation Results

The result of SPICE simulation based on 0.35$\mu$m standard CMOS technology is shown in Figures 5 and 6. The transistors sizes are reported in the table 1. A supply voltage of 2V is used. Figure 5 shows simulation result for the circuit from figure 2. In this case the circuit is used as a current squarer where $I_X$ is multiplied by itself and divided by $I_\sigma$. The relative error of the simulation result shown in Fig. 5 is less than 2.8%.

Fig. 6 depicts the obtained curves of the Gaussian circuit compared to half Gaussian function. The maximum power consumption is of 8.5 microwatts.

6 Conclusion

A simple circuit that implements a Gaussian function has been proposed. The input current is squared and converted to voltage and MOS transistor in weak inversion then performs the exponential function. The simulation results show a very good approximation of true Gaussian function. The proposed circuit is characterized with very low power consumption. The circuit is suitable to be used in many analog signal processing blocks to perform neural algorithms.

References


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